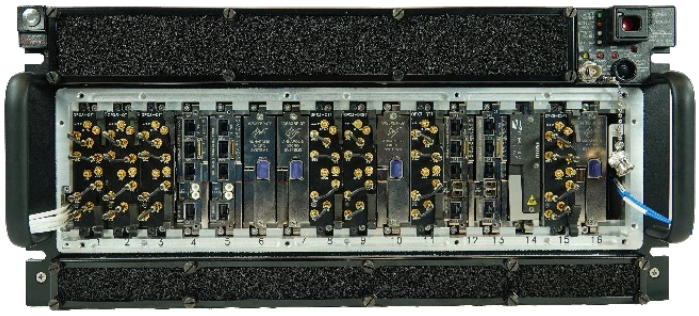
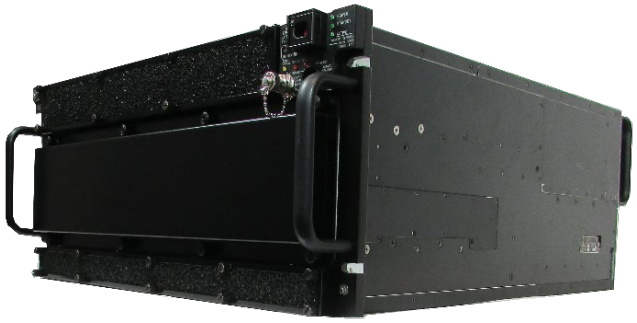
Digital Receiver Technology, Inc.

DRT OpenVPX Modular Products Family
DRT1712

Aligned with CMOSS and SOSA™ specifications



DRT1712 without Cover



DRT1712 with Cover

DRT OpenVPX – DRT's Next Generation SDR Product Line

The DRT OpenVPX products family comprise the next generation DRT Software-Defined Radio (SDR) hardware and software products, and mission capabilities. These are defined according to the Modular Open Systems Approach (MOSA) in alignment with the CMOSS/SOSA™ architecture. The C5ISR Modular Open Suite of Standards (CMOSS) and the Sensor Open Systems Architecture (SOSA) specify common open standards for interoperability and interchangeability between vendor components.

DRT OpenVPX chassis and plug-in cards (PIC) apply OpenVPX HW and SW standards in alignment with CMOSS/SOSA to ensure DRT OpenVPX PICs can be utilized in other vendor chassis, and to ensure that other vendor PICs can be utilized in a DRT OpenVPX chassis. DRT OpenVPX chassis and PICs include a Software Development Kit (SDK) to facilitate third party application integration with DRT OpenVPX SDRs. DRT's Orion Software Framework uses the DRT OpenVPX SDKs for mission applications integration. (See the *Orion Software Framework & Mission Applications* data sheet to learn more about DRT OpenVPX software and system capabilities.)

DRT PICs may be used in third party chassis and DRT applications may be hosted on third party hardware, although integration and licensing fees may apply. Contact DRT for additional information.

The DRT1712, the first in DRT's OpenVPX Product Line, provides up to twice the signal processing capacity and almost 20 times the digital signal data offload capacity as a DRT12C MAX system. The OpenVPX SDR hosts DRT-provided signal processing applications for intercepting Cellular, Wi-Fi, Push-To-Talk (PTT), Frequency Hopped Spread Spectrum (FHSS) and for geolocation of the same. In addition to the organic signal processing applications, the DRT OpenVPX SDR egress and ingress data pipes enable offboard processing by one or more external servers.

DRT1712 DESCRIPTION

The DRT1712 is a CMOSS/SOSA chassis with a 16 slot 100 Gbps 3U OpenVPX backplane that is populated with DRT OpenVPX and third party 3U OpenVPX PICs. The DRT1712 backplane has 12 CMOSS payload slots, each can be factory provisioned for 4 channels of RF I/O, to support RF tuner and signal processing cards. The backplane also has 4 switch slots, each supporting 600 Gbps of full duplex, non-blocking, digital signal data I/O that can be provisioned with an AMS switch that supports 300 Gbps of full duplex optical Ethernet I/O.

KEY FEATURES and SPECIFICATIONS

Unparalleled RF Density with Flexible Configuration Options: A DRT OpenVPX SDR with 12 DRT OpenVPX 4 channel tuner cards (QT1 or QT1-FE) and 4 AMS switch cards can receive, digitize, decimate, down convert, and offload IQ for a wide variety of wide and narrow RF bandwidths and sample rates.

Rev. 1.3, November 2024, X24-00182-000

NOT APPROVED FOR PUBLIC RELEASE

- Up to 48 500 MHz RF bandwidth channels offloaded at 640 Msps per channel in V49.2 packets
  - Between 1.5 MHz and 18 GHz, up to 44 GHz from DF antennas with downconverters
  - Max 24 GHz of bandwidth for stare, beamforming, and DF applications
  - Max 1.2 Tbps V49.2 wideband IQ packet streaming offload over Ethernet
  - DRT's QT1, QT1-FE, DXR1, and DXR1-FE can also be configured to receive 40, 80, and 500 MHz RF bandwidths
- Up to 96 wideband V49.2 IQ streams offload in combinations of 80, 96, 160, 320 and 640 Msps that do not exceed 1.2 Tbps max
  - Each 500 MHz RF channel can be decimated into 2 IQ streams of independent rates
  - The 96 Msps IQ rate, for 80 MHz, eases porting DRT12C capabilities to DRT OpenVPX systems
- About 100 Narrowband DDCs per QT1 with a wide range of bandwidths and sample rates
- Compare DRT 12C systems:
  - Max 72 x 40 MHz analog channels in a 12C offload only system
  - Max 32 x 40 MHz digital channels for a 12C MAX system with V49 offload

Signal Processing Intensive: The DRT1712 can also be provisioned with a variety of signal processing cards (SBC/GPP, FPGA, GPUs) to host DRT 12C signal processing applications.

- Provide twice the signal processing capacity as a DRT12xxC MAX signal processing system
- V49.2 IQ streams can be addressed for concurrent in-chassis processing and offload

Modular Open Systems Approach (MOSA): The DRT1712 is designed according to principles of modularity and openness in alignment with CMOSS and SOSA.

- SOSA Reference Architecture 1.0 Aligned
- CMOSS Designated OpenVPX Slot Profiles
  - Payload Slot Profile: SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11-4 (aka 14.16.11-4)
  - Switch Slot Profile: SLT3-SWH-6F8U-14.4.15 (aka 14.4.15)
- OpenVPX and associated standards
  - VITA 46.0 – VPX Baseline Standard
  - VITA 46.11 – System Management on VPX
  - VITA 48.2 – Mechanical Standard for VPX REDI Conduction Cooling
  - VITA 49.2 – VITA Radio Transport (VRT) Standard for Electromagnetic Spectrum
  - VITA 65.0 – OpenVPX System Standard
  - VITA 65.1 – OpenVPX System Standard – Profile Tables
  - VITA 67.3 – Coaxial Interconnect on VPX, Spring-Loaded Contact on Backplane

Backplane for Capability Density: The DRT1712 backplane was designed to maximize the number of slots in a 19" rack mount chassis to maximize capability density.

- 16 x OpenVPX Slots
  - 12 x Payload Slots w/ VITA 67.3c RF apertures with 4 x RF I/O + 100 MHz RF Reference In
  - 4 x Switch Slots with 8 Control Plane Ports + 6 Full Duplex 100 Gbps Data Ports
  - 3U high x 1" pitch (wide) per VITA 46.0
  - Conduction Cooled per VITA 48.2
- OpenVPX Backplane Connectivity
  - Control Plane (10-25 Gbps Ethernet) - Victory Data Bus (VDB)
  - Data Plane (100 Gbps Ethernet) - MORA Low Latency Data Bus (ML2B)
  - Switched Expansion Plane (100 Gbps Ethernet)
  - Pairwise Slot-Slot Expansion Planes (100 Gbps PCIe, Aurora, or Ethernet)
  - Management Plane – IPMI/IPMB per VITA 46.11 VPX System Management
  - Maintenance Ports (2 per payload slot, 1 per switch slot)
  - Sync Lines (2 per payload slot)
- Proven Interoperability with OpenVPX 3U Plug-in Cards (PIC)
  - DRT OpenVPX - QT1 Quad-Tuner – see DRT OpenVPX-QT1 data sheet
  - DRT OpenVPX - QT1-FE Frequency Extended Quad Tuner – see DRT OpenVPX-QT1-FE data sheet
  - DRT OpenVPX - DXR1 Dual Transceiver w/ 2 Rx and 2 Tx channels – see DRT OpenVPX-DXR1 data sheet
  - Annapolis Micro Systems - WP3E10 3U OpenVPX Switch
  - Annapolis Micro Systems - WB3XBP 3U OpenVPX Virtex Ultrascale FPGA Processor
  - Mercury - RFM3113 Ultra-Wideband Microwave Dual Up Converter
  - Kontron - VX305H-40G OpenVPX Compute Intensive SBC
  - Abaco SBC3612D OpenVPX Compute Intensive SBC
  - Wolf 144L NVIDIA RTX™ GA104 GPU accelerator Red Rock SOSA-Aligned Storage Card with Removable SSD

Infrastructure for Capability Density: The DRT1712 places infrastructure functions such as PNT, chassis management and peripheral interface management behind the backplane so that backplane slots are dedicated to maximizing capability density.

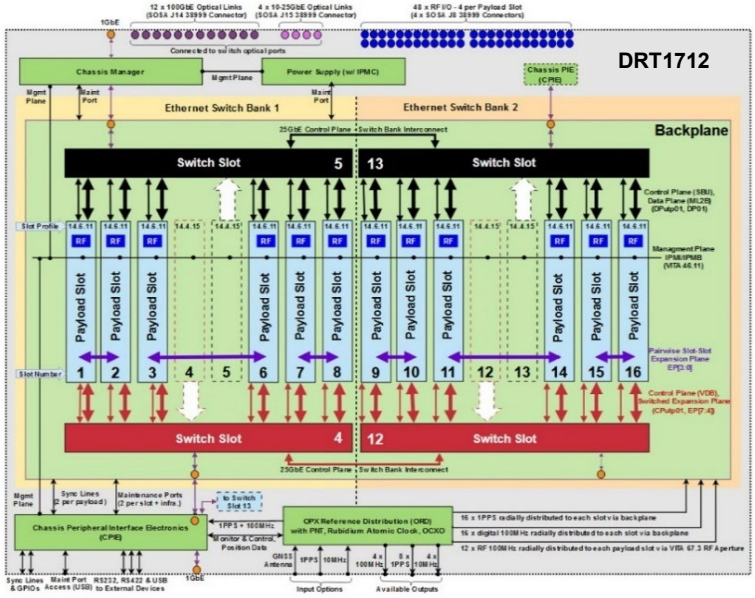
- PNT with TFNG compliant reference generation and distribution
  - Rubidium atomic clock for superior hold-over
  - GNSS 1PPS disciplined low phase noise OCXO for 100 MHz reference
  - 1PPS and 100 MHz OpenVPX reference clocks radially distributed via backplane
  - 100 MHz RF reference direct to each payload slot via VITA 67.3 RF aperture
- Chassis Management
  - Chassis Manager w/ IPMI over IPMB to IPMCs and IPMI over Ethernet to System Manager
  - Intelligent Platform Management Controllers (IPMC) in PICs and Infrastructure
  - VITA 46.11 VPX System Management
  - SOSA Tier 2, some Tier 3
- Peripheral Management
  - Chassis Peripheral Interface Electronics (CPIE)
  - 1 to N Sync Line Distribution between internal and external SDR components
  - Maintenance Port access all processors, IPMCs and Chassis Manager
  - Navigational data distribution via Ethernet (NMEA, V49.2, VICTORY)
  - External devices: up to 4 RS232, up to 2 RS422 and 1 USB serial interfaces
- Power Consumption
  - 28V DC nominal between 22 min and 33 max VDC
  - 1500 Watts maximum recommended via only SJ1 input power connector
  - 1800 Watts maximum for fully loaded with 75 Watts per slot
  - 2200 Watts maximum for fully loaded with 100W per Slot and 5°C reduced ambient temp
  - For greater than 1500W, recommend input power via both SJ1 and SJ6 connectors

Other Specifications:

- Weight
  - Empty Chassis: 75 lbs
  - Fully Loaded Chassis: 110 lbs
- Operating Temperature (ambient): -20°C to +50°C (-4°F to +122°F), +45°C w/ 100W per slot
- Dimensions:
  - Width: 17 in. (43.18 cm), 19” rack mountable
  - Height: 5U – 8.75 in. (22.23 cm)
  - Depth: 26.18” from front mounting surface to extent of rear handles

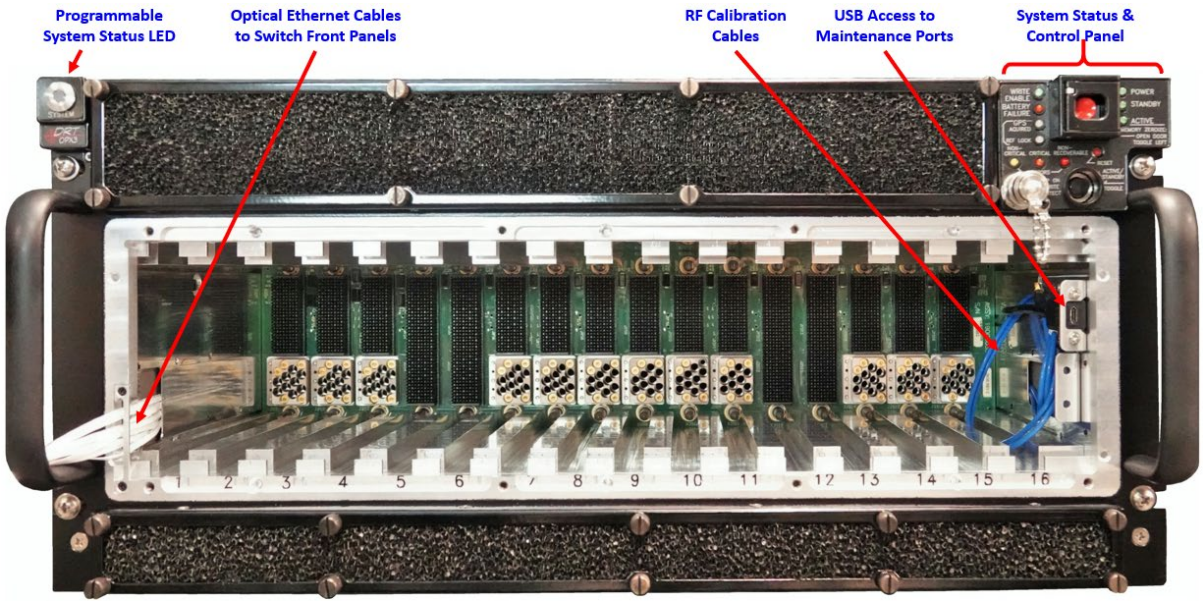
DRT1712 Slots, Backplane, and Chassis Connectivity

The following diagram illustrates the DRT1712 backplane topology, infrastructure components and other elements of the DRT1712 that are mentioned in the Key Features section.

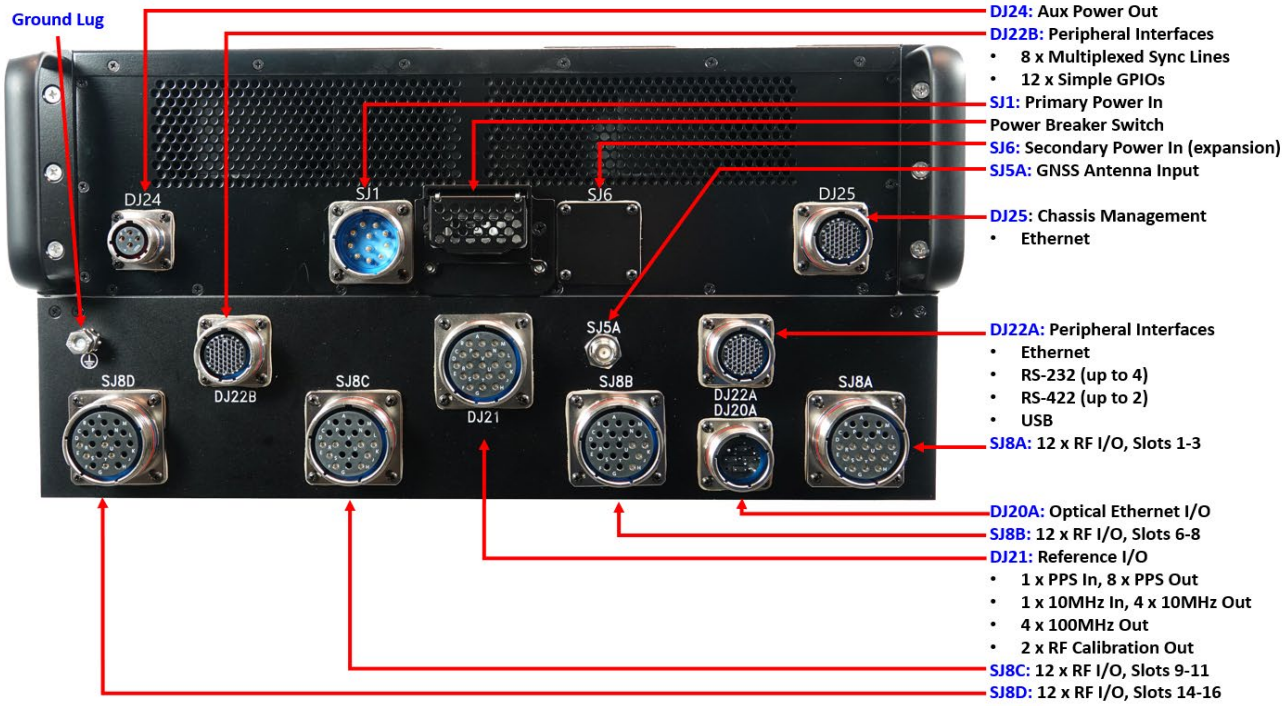


Not subject to US Export Administration Regulations (15 C.F.R. Parts 730-774) or US International Traffic in Arms Regulations (22 C.F.R. Parts 120-130).

Rev. 1.3, November 2024



DRT1712 Chassis Front View



DRT1712 Chassis Rear View

Not subject to US Export Administration Regulations (15 C.F.R. Parts 730-774) or US International Traffic in Arms Regulations (22 C.F.R. Parts 120-130).

12409 Milestone Center Drive, Germantown, MD 20876-7114
Phone: 301-916-5554 ~ www.drti.com ~ info@drti.com

Rev. 1.3, November 2024